Fault Elimination In Transmission Line Using Eleven Level Statcom

student details:
name: davu.srinivasa rao
rollno: 09a01d4310
nova college of engg & technology
vegavaram, jangareddigudem,
westgodavari, andhra pradesh
ph no:0949134848
email: sri.davu@gmail.com

***abstract*— this paper we deals with a simultaneous compensators (statcoms) uses several levels converters as: a) lower harmonic injection into the power system; a) decreased stress on the electronic components due to decreased voltages; and c) lower switching losses. one unfavorable, however, is the increased likelihood of a switch failure due to the increased number of switches in a several levels converter. a single switch failure, however, does not necessarily force a (2*n* + 1)-level statcom offline. even with a decreased number of switches, a statcom can still supply a significant range of control by removing the module of the not working switch and continuing with (2*n* − 1) levels. in this paper shows an approach to detect the existence of the not working switch, identify which switch is not working, and reconfigure the statcom. this approach is illustrated on an eleven-level statcom and the effect on the dynamic performance and the total harmonic distortion (thd) is analyzed.**

I. introduction

in this paper static simultaneous compensators (statcom) have been well accepted as a power system controller for increasing voltage regulation and reactive compensation [1]–[5]. it contains several compelling reasons to consider a several levels converter topology for the statcom [6]–[8]. these lknown reasons include the following: 1) lower harmonic injection into the power system; 2) decreased stress on the electronic components due to decreased voltages; and 3) lower switching losses [9]. various several levels converters also readily lend themselves to a variety of pwm strategies to improve efficiency and control. an eleven-level cascaded several levels statcom is shows in fig. 1. this converter uses several full bridges in series to synthesize staircase waveforms. because every full bridge can having three output voltages with different switching combinations, the number of output voltage levels is 2*n* + 1 where *n* is. the number of full bridges in every phase. the converter cells are identical and therefore modular

as higher level converters are used for high output rating power applications, a large number of power switching devices

Guide details:
name:k.ratnaraju,
associate professor, eee department,
nova college of engg & technology,
vegavaram, jangareddigudem,
westgodavari, andhra pradesh
ph no: 9704195580
email: ratnaraju.11@gmail.com

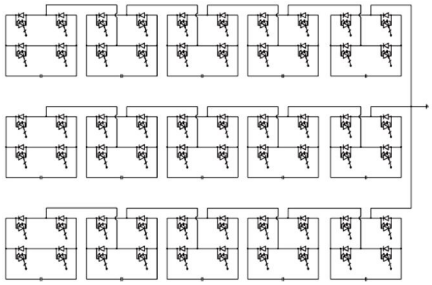


fig. a. eleven-level cascaded several levels statcom.

will be used. each of these devices is a potential failure point. therefore, it is important to design a sophisticated control to produce a fault-tolerant statcom. a faulty power cell in a cascaded h-bridge statcom can potentially cause switch modules to explode [10] leading to the fault conditions such as a short circuit or an overvoltage on the power system resulting in an expensive down time [11]. subsequently, it is crucial to identify the existence and location of the fault for it to be removed.

several fault elimination methods have been proposed over the last few years [10]–[18]. resistor sensing, current transformation, and v_{ce} sensing are some of the more common approaches. for example, a method based on the output current behavior is used to identify igbt short circuits [12]. the primary drawback with the proposed approach is that the fault elimination time depends on the time constant of the load. therefore,
for loads with a large *rl* time constant, the faulty power
cell can go undetected for numerous cycles, potentially leading to circuit damage. another fault elimination approach proposed in [13] is based on a switching frequency analysis of the output phase voltage. this method was applied to flying capacitor converters and has not been extended to cascaded converters. ai-based methods were proposed to extract pertinant signal features to detect faults in

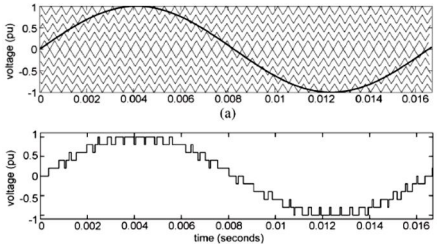
[14]. in [15], sensors are used to measure each igbt current and to initiate switching if a fault is detected. a fault-tolerant neutral point-clamped converter was proposed in [16]. in [17], a reconfiguration system based on bidirectional switches has been designed for three-phase asymmetric
cascaded h-bridge inverters. the fundamental output
voltage phase shifts are used to rebalance a faulted several levels cascaded converter in [18].in this paper, the method we propose requires only that the output dc link voltage of each phase be measured. this measurement is typically accomplished anyway for control purposes. if a fault is detected, the module in which the fault occurred is then isolated and removed from service. this approach is consistent with the modular design of cascaded converters in which the cells are designed to be interchangeable and rapidly removed and replaced. until the module is replaced,
the several levels statcom continues to operate with slightly decreased, but still acceptable, performance.
in summary, this approach offers the following advantages:

1. no additional sensing requirements;
2. additional hardware is limited to two by-pass switches per module;
3. is consistent with the modular approach of cascaded several levels converters; and
4. the dynamic performance and thd of the statcom is not significantly impacted.

ii. several levels statcom
a cascaded several levels statcom contains several h-bridges in series to synthesize a staircase waveform. the inverter legs are identical and are therefore modular. in the eleven-level statcom, each leg has five h-bridges. since each full bridge generates three different level voltages (v, 0,$-v$) under different switching states, the number of output voltage levels will be eleven. a several levels configuration offers several advantages
over other converter types [19].
a) it is better suited for high-voltage, high-power applications than the conventional converters since the currents and voltages across the individual switching devices are smaller.
b) it generates a multistep staircase voltage waveform approaching a more sinusoidal output voltage by increasing the number of levels.
c) it has better dc voltage balancing, since each bridge has its own dc source.

to achieve a high-quality output voltage waveform, the voltages across all of the dc capacitors should maintain a constant value. variations in load cause the dc capacitors to charge and discharge unevenly leading to different voltages in each leg of each phase. however, because of the redundancy in switching states, there is frequently more than one state that can synthesize any given voltage level. therefore, there exists a "best" state among all the possible states that produces the most balanced voltages [20]. since there are multiple possible switching states that can be used to synthesize a given voltage level, the particular switching topology is chosen such that the capacitors with the lowest voltages are charged or conversely, the capacitors with the highest voltages are discharged. this redundant state selection approach is used to maintain the total
dc link voltage to a near constant value and each individual cell capacitor within a tight bound.

different pulse width modulation (pwm) techniques have been used to obtain the several levels converter output voltage. one common pwm approach is the phase shift pwm (pspwm) switching concept [21]. the pspwm strategy causes cancella-



(1)

fig. d. (1) carrier and reference waveform for pspwm. (2) output waveform.

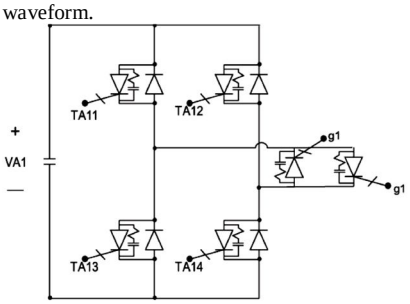


fig. c. cell with fault switch.

tion of all carrier and associated sideband harmonics up to the(n − 1)th carrier group for an n-level converter. each carrier signal is phase shifted by

$$\Delta_{\emptyset} = \frac{2\pi}{n}$$

where n is the number of cells in each phase. fig. 2 illustrates the carrier and reference waveforms for a phase leg of the eleven-level statcom. in this figure, the carrier frequency has been decreased for better clarity. normally, the carrier frequency for pwm is in the range of 1–10 khz.
iii. fault analysis for the several levels statcom

a converter cell block, as shown in fig. 3, can experience several types of faults. each switch in

the cell can fail in an open or closed state. the closed state is the most severe failure since it may lead to shoot through and short circuit the entire cell. an open circuit can be avoided by using a proper gate circuit to control the gate current of the switch during the failure [23]. if a short circuit failure occurs, the capacitors will rapidly discharge through the conducting switch pair if no protective action is taken. hence, the counterpart switch to the failed switch must be quickly turned off to avoid system collapse due to a sharp current surge. nomenclature for the proposed method is given in table i.

table 1

E_{out}	satcom output voltage(v)
E_{out}	filtered satcom output voltage (rms)(v)
E'	SATCOM thereshold voltage constant)(v)
$s_{j1}s_{j2}$	Switching signal of the i-th cell(0,1)
f_i	Possible between possible and actual sitcom output (v)
x_i	Difference between possible and actual STATCOM OUTPUT(V)
g_i	bypas signal for j-th cell (0,1)

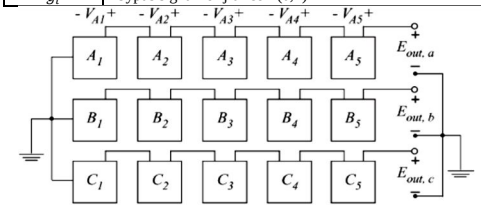


fig. d. simplified eleven-level cascaded several levels statcom.

the staircase voltage waveform shown in fig. 2 is synthesized by combining the voltages of the various cells into the desired level of output voltage. at the middle levels of the voltage waveform, due to the switching state redundancy, there are more than one set of switching combinations that may be used to construct the desired voltage level. therefore, by varying the switching patterns, the loss of any individual cell will not significantly impact the middle voltages of the output voltage. however, the peak voltages require that all cells
contribute to the voltage; therefore, the short circuit failure of any one cell will lead to the loss of the first and (2*n* + 1) output levels and cause degradation in the ability of the statcom to produce the full output voltage level.

consider the simplified eleven-level converter shown in fig. 4. the process for identifying and removing the faulty cell block is summarized in fig. 5. the input to the elimination algorithm is $\hat{e}_{out}$ for each phase, where $\hat{e}_{out}$ is the statcomfiltered rms output voltage. if the statcom rms output voltage drops below a preset threshold value (e_), then, a fault
is known to have occurred (see fig. f).

once a fault has been detected to have occurred, then, the next step is to identify the faulty cell. by utilizing the switching signals in each converter cell, (i.e., s_1 and s_2), it is possible to calculate all of the possible voltages that can be produced at any given instant as illustrated in table ii (terminology adopted
from [23]):

thus, the output voltage of a cell is

$$v_{ax} = v_{ax} + -v_{ax} \quad (1)$$

and since the cells of the statcom are serially connected, the total output voltage per phase is

$$v_{yo} = \sum_{x=1}^{n} v_{yx} \; y \in [a, b, c]$$

where *n* is the number of blocks.

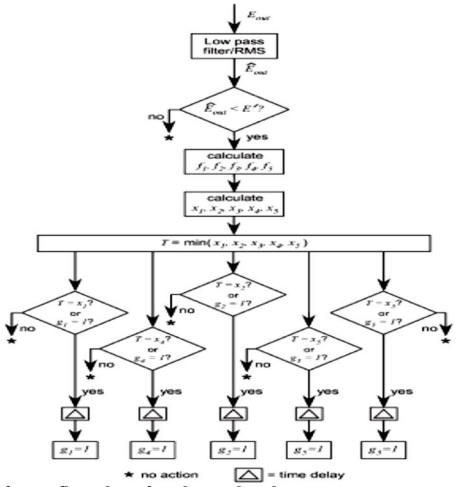


fig. e. flowchart for eleven-level converter.

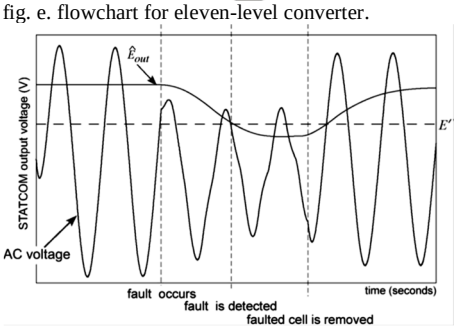


fig. f. statcom-filtered output voltage and threshold value.

by utilizing the switching signals in each converter cell,
(i.e., s_{j1} and s_{j2}, j is the cell number), it is possible to
calculate all of the possible voltages that can be produced at any

table ii

S_1	S_2	v_{ax}^{+}	v_{ax}^{-}	v_{ax}
0	0	0	0	0
0	1	0	v_{dc}	$-v_{dc}$
1	0	v_{dc}	0	v_{dc}
1	1	v_{dc}	v_{dc}	0

Switching State and Output Voltage of an h-bridge

given instant. when there is a fault in the several levels converter, the capacitor at the faulty block will rapidly discharge. this discharge results in a phase shift in the output ac voltage as well as a change in amplitude of voltage. the set of all possible phase fault voltages for an eleven-level converter is given by

f_1=v_{dc0} ($s_{21} - s_{22} + s_{31} - s_{32} + s_{41} - s_{42} + s_{51} - s_{52}$)
(cell 1 faulted)

f_2=v_{dc0} ($s_{11} - s_{12} + s_{31} - s_{32} + s_{41} - s_{42} + s_{51} - s_{52}$)
(Cell 2 faulted)

:

f_5=v_{dc0} ($s_{11} - s_{12} + s_{21} - s_{22} + s_{31} - s_{32} + s_{41} - s_{42}$)

(Cell 5 faulted)
Where v_{dc0} is the ideal voltage across a single cell block.
if there is a faulted cell, only one f_i will be near the actual
statcom output phase voltage e_{out}; all of the others will be too high. Therefore, to determine the location of the fault cell, each f_i is compared against e_{out} to yield
$x_i = |e_{out} - f_i|, i = 1, \ldots, n.$ (4)
the smallest x_i indicates the location of the faulted block
because this indicates the f_i which most closely predicts the actual e_{out}.
the choice of threshold voltage $e_{\_}$ depends on the number of cells in the converter. the ideal output voltage is

$$\hat{E}_{out,o} = \frac{nv_{dco}}{\sqrt{2}} \quad (5)$$

during a fault, e_{out} will decrease by v_{dc0} yielding

$$\hat{E}_{out,fault} = \frac{(n-1)v_{dco}}{\sqrt{2}} = \frac{(n-1)}{n}\hat{E}_{out,o} \quad (6)$$

therefore, the threshold voltage $e_{\_}$ should be chosen such that $(n - 1/n)e_{out,0} \leq e_{\_} \leq e_{out,0}$. in an eleven-level converter, $n = 5$ and the faulted rms voltage will decrease by roughly 20%. therefore, a good choice for $e_{\_}$ is 85% of the rated output statcom voltage.
the last step is to actuate the module bypass switch g_i shown in fig. c. a slight time delay is added to the logic to neglect for momentary spikes that may occur. it is desirable to neglect momentary sags in the dc link voltage, but respond to sags of increased duration that indicate a faulted module. fig. g shows the realization logic for the proposed fault elimination and module
removal method.

the use of a fault handling switch in several levels converters is not uncommon. in [26], a fault handling switch is used in a flying capacitor several levels inverter. while the additional circuitry
does increase the cost of the circuit, it also increases the reliability be enabling the circuit to keep working (albeit at a slightly decreasedd operating range) until the module can be replaced.

iv. example and results

the single line diagram of the electrical distribution system feeding an arc furnace is shown in fig. 8. the statcom has been shown to be an efficient controller to mitigate arc furnace flicker [27]. the electrical network consists of a 115-kv generator and an impedance that is equivalent to that of a
large network at the point of common coupling (pcc). the statcom is connected to the system through a y-delta transformer. the system was simulated using pscad/emdtc. the electrical arc furnace load is nonsinusoidal, unbalanced, and randomly fluctuating. electric arc furnaces are typically used to melt steel and will produce current harmonics that are random. in addition to the integer harmonics, arc furnace
currents are rich in interharmonics [24]. the flicker waveform has subseveral levels variations in the 5–35-hz range [25]. fig. ishows the active power drawn by the arc furnace. note that the statcom is able to improve the line active power such that active power variations caused by the arc furnace do not propagate throughout the system as shown in fig.j. the simulation model and control scheme is described in detail in [28]. the dc capacitor voltages normally vary and are kept in
relative balance through redundant state selection [20].

a. dynamic performance

to test the proposed fault elimination and mitigation approach, a faulty switch was initiated at 2.5 s. within 300 ms, the fault has been detected, the module removed, and the statcom restored to steady-state operation. this fault duration is longer than is necessary; the fault was intentionally left on to better illustrate its effect on the system and removal. the statcom bus voltage and line active powers are shown before the fault, during, and after the faulty module is removed (figs. k
and l). note that both the bus voltage and line active power are adversely affected during the fault. in both cases, the highfrequency oscillations are increased. once the faulty module is removed, the system returns to its prefault behavior. there is a small induced low-frequency oscillation that can be observed in the line active power, but this is rapidly damped by the
statcom's control.
the average dc link voltage before, during, and after the
fault is shown in fig. m. during the fault, the dc voltage
drops rapidly as the faulted module capacitor discharges.when the faulty module is removed, the
average dc voltage drops to roughly 80% of the initial voltage, as expected. the continued variation in the dc link voltage is due to the continual variation of the arc furnace load that the statcom is compensating and
is normal.

fig. g. proposed fault elimination and remediation control for cell 1.

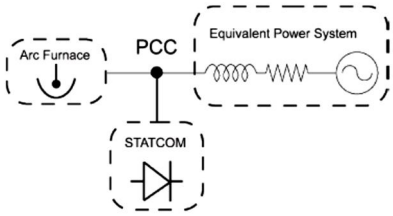


fig. h. test system.

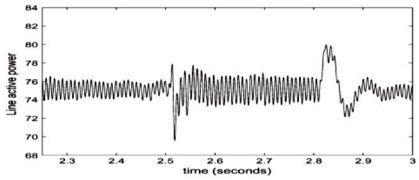


fig. l. line active power before, during, and after fault.

fig. 14 shows two cycles of the statcom several levels voltage output. there are several important aspects of this output waveform that have been highlighted. first, note the voltage collapse of the first level due to the faulted cell. this collapse in voltage will occur at the level that corresponds to the faulty cell. it is not possible to directly correlate the level number with the cell number (i.e., a collapse in level four does not necessarily
indicate a fault in cell 4) because of the redundant state selection scheme that is used to balance the capacitor voltages.

a further aspect of note is the increase in length of the toplevel duration. this is due to the increase in the modulation gain k due to the decrease in dc link voltage. since the statcom output voltage is directly proportional to

$v_{stat} = kv_{dc} \cos \alpha$

where k is the modulation gain and α is the phase angle.

if v_{dc} decreases by 20%, then, k must increase by 20% to
compensate. an increase of this magnitude in odulation gain takes thepwminto overmodulation where the magnitude of the reference waveform exceeds the magnitude of the carrier. this results in an increased length of time at higher voltage levels. overmodulation may also result in the increase of lower frequency
harmonics. the modulation gain k is shown in fig. 15.

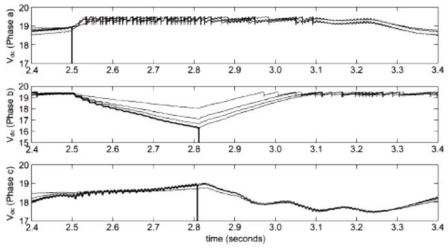
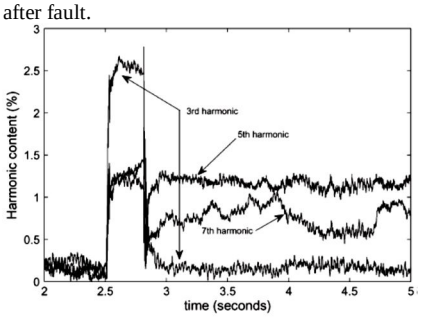


fig. 16. individual module capacitor voltages before, during, and after fault.



during, and after fault.

the individual module capacitor voltages in each phase for a faulty *a* phase switch are shown in fig. 16. note that the faulted module voltage decays rapidly at 2.5 s (when the fault was applied). the remaining capacitor voltages in phase *a* show significant "chopping" as the redundant state selection
approach rapidly alternates between modules to maintain the average dc link voltage. a crowbar circuit is used with each module to limit the maximum dc voltage, leading to the chopping behavior. phase *b* shows a continual decline in all of the capacitor voltages until the corresponding faulty module is removed at 2.8 s. the capacitor voltages increase until they are in the nominal range and then exhibit similar "chopping" until they are regulated. phase *c* does not exhibit chopping because
all of the individual cell voltages are of similar magnitude and do not exceed the crowbar maximum.

b. thd performance

harmonic injection is a concern with statcoms [29]. a harmonic analysis has been performed on the output voltage at the point of common coupling. one of the primary reasons for using a several levels converter is the reduction in harmonic content in the output waveform. fig. 17 shows the harmonic distortion levels at the statcom pcc before, during, and after the fault. since this is measured at the pcc, the output waveform has already been filtered to remove high-frequency

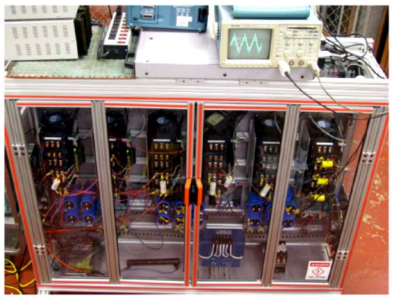


fig. 18. experimental statcom.

components. before the fault, the thd level is less than 1%, which is quite good. during the fault, the thd increases to over 5%. when the fault is removed, the thd decreases and settles at approximately 2.5%, which is in the acceptable range for a 115-kv system [30]. therefore, the loss of one of the cells does not necessitate the immediate removal of the statcom
from service. the increase in thd after removing the faulty cell is due to several reasons. first, the statcom filters were tuned to the resonant frequencies associated with the elevenlevel converter and are not as effective when the converter topology changes to a 9-level. second, the over modulation required for the 9-level

converter increases the content of the lower frequency harmonics. while the third harmonic is quite
high during the fault, it returns to prefault levels after the fault is cleared, whereas the fifth and seventh remain fairly high due to the overmodulation. even though they are increased over the prefault value, they still remain under the 1.5%-limit required of 115-kv systems [30].

v. Experimental Results

to confirm the operation of the fault elimination algorithm
for cascaded h-bridge several levels converters, an experimental prototype is constructed for applying and detecting different type of faults. the laboratory prototype of the statcom converter is shown in fig. 18. the experimental rack consists of 36 powerex cm75du-24f igbts rated at 1200 v and 75 a for main switching devices. passive components include a 1.2-mh, 45-a reactor and 18 electrolytic capacitors rated at 3900 μf and 450 v. the igbts are driven by a concept 6sd106e1 gate drivers and controlled by a 320f2812 fixed-point digital signal processor (dsp).

for this prototype, three h-bridge cells are cascaded to make a seven-level inverter for each phase of the statcom. during normal operation, the capacitor voltage for each cell is 30 v. a tms320f2812 dsp is used for the calculation of the modulation, control, and fault elimination algorithms. the h-bridges are constructed from the igbts switches and the gate signals
of the igbts are delivered via fiber optic cables.

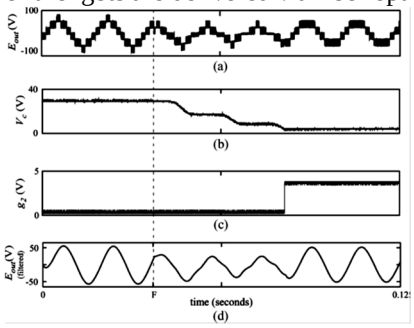


fig. 19. experimental statcom dynamics before, during, and after a fault is applied; (a) *e*out, (b) capacitor voltage at faulted cell, (c) gating signal of cell 2 by-pass switch, and (d) *e*out (filtered).

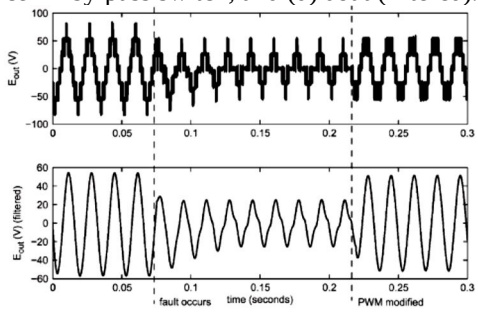


fig. 20. experimental statcom dynamics showing change in pwm.

the output voltage of the converter during the normal operation, during the fault, and after removing the faulty cell is depicted in fig. 19(a). a fault is applied to the second cell at point "f" as shown in the figure with the dashed line. immediately after the fault is applied, the block capacitor begins to discharge. the capacitor voltage is shown in fig. 19(b) . fig. 19(c) shows the output of the fault elimination algorithm.
when a fault is detected, g_2 (the gate signal of the by-pass circuit) becomes activated and it triggers the by-pass of the second cell and deactivates the pwmcommands to the faulty h-bridge. fig. 19(d) shows the filtered output of the statcom. note that the amplitudes of the sinusoidal waveforms are nearly identical before and after fault elimination and bypass. after detecting the fault and bypassing the faulty h-bridge, the modulation index is increased to compensate for the lost voltage levels in the output. in addition, the pwm switching patterns are modified based
on existence of two cascaded h-bridges instead of three. this causes significant improvement in the output waveform of the converter.

fig. 20 shows the same fault as in fig. 19, except the fault bypass signal is intentionally delayed by several cycles to

TABLE 3
Fault identification methods

Method	Requires	Computation complexity	Detection requirement
Voltagefrequency analysis	Voltage angle	Complex frequency analysis	less than 1 cycle
Ai-based fault detection	Voltage magmitude	Requires NN training	About 6 cycles
Proposed method	Voltage magmitude	Simple caculations	About 1 cycle

demonstrate the effect of changing the pwm pattern. note that after the fault and discharge of the corresponding capacitor, the output waveform contains considerable distortion. however, modifying the pwm switching signals based on two cascaded h-bridges, the thd of the output waveform can be significantly
decreased and the filtered output waveform become sinusoidal again.

vi. Method Comparisons

each fault elimination method has its own advantages and
disadvantages.most of the methods in the literature are applicable to neutral point-clamped converters and are therefore not directly applicable to cascaded converters. in this section, each applicable approach is succinctly summarized and compared with other methods. two recent methods are briefly reviewed below.

a) **voltage frequency analysis** [23]. in this scheme, the
basic approach is to use spwm to produce the converter
output voltage. by using spwm, voltages with different

phase angles will be produced at each cell of the several levels converter. the sum of the three phase voltages is zero in normal operation, but that is not zero if there is
a faulty cell. this condition is used as the criteria for identifying the faulty cell. the phase angle of the voltage
sum indicates the location of the fault.
b) **ai-based fault elimination** [14]. this scheme is built
around a neural network (nn) classification for fault diagnosis of an several levels cascaded converter. multilayer
perceptron networks are used to identify the type and
location of occurring faults. the principal component
analysis is utilized in the feature extraction process to
decreased the nn input size.

since these methods are all designed to detect and then bypass the faulted cell, the hardware requirements are identical. these methods are compared and contrasted to the proposed method in table iii.
each method has its own advantages and disadvantages. for
example, the voltage frequency method detects and clears the faulty cell rapidly, but requires complex frequency analysis and may not be suitable for implementation in all applications. the proposed method does not respond as rapidly, but only requires simple calculations and can be implemented easily in most
dsps. furthermore, the proposed method only requires voltage magnitude measurements which are easily obtained.

vii. Conclusion

in this paper, a fault elimination and mitigation strategy for
a several levels cascaded converter has been proposed. this approach requires no extra sensors and only one additional bypass switch per module per phase. the approach has been validated on a 115-kv system with a statcom compensating an electric arc furnace load. this application was chosen since the arc furnace provides a severe application with its nonsinusoidal, unbalanced, and randomly fluctuating load. the
proposed approach was able to accurately identify and remove the faulted module. in addition, the statcom was able to remain in service and continue to provide compensation without exceeding the total harmonic distortion allowances.

References

[1] v. dinavahi, r. iravani, and r. bonert, “design of a real-time digital
simulator for a d-statcom system,” *ieee trans. ind. electron.*, vol. 51,
no. 5, pp. 1001–1008, oct. 2004.
[2] b. singh, s. murthy, and s. gupta, “statcom-based voltage regulator
for self-excited induction generator feeding nonlinear loads,” *ieee trans.*
ind. electron., vol. 53, no. 5, pp. 1437–1452, oct. 2006.
[3] a. luo, c. tang, z. shuai, j. tang, x. xu, and d. chen, “fuzzy-pi-based
direct-output-voltage control strategy for the statcom used in utility
distribution systems,” *ieee trans. ind. electron.*, vol. 56, no. 7, pp. 2401–
2411, jul. 2009.
[4] m. molinas, j. suul, and t. undeland, “extending the life of gear box in
wind generators by smoothing transient torque with statcom,” *ieee*
trans. ind. electron., vol. 57, no. 2, pp. 476–484, feb. 2010.