Design of a Multiplexer In Multiple Logic Styles for Low Power VLSI

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***Abstract* -The Low power and low energy has become an important issue in today's consumer electronics. Any combinational circuit can be represented as a multiple inputs with single output. Multiplexers are used to design any digital combinational logic circuit. Hence it is required to design a multiplexer with low power consumption and high speed. The main objective of this paper is to design the multiplexer using complementary metal oxide semiconductor (CMOS) logic and pass-transistor logic styles.The power consumption, delay, area, transistor count of various logic styles are compared. This paper shows that static NMOS logic multiplexer is an optimum device level design which has characteristics of high speed with minimum power compared with other realizations. These different logic styles are compared by performing detailed transistor level simulations using CAD tools of DSCH3 and Micro wind 3.1 in submicron regime.**

***Keywords* - CMOS, Low power, High Speed, Area**

I. INTRODUCTION

The increasing demand for low-power very large scale integration (VLSI) can be addressed at different design levels, such as the architectural, circuit, layout, and the process technology level. At the circuit design level, considerable potential for power savings exists by means of proper choice of a logic style for implementing combinational circuits. This is because all the important parameters governing power dissipation, switching capacitance, transition activity, and short-circuit currents are strongly influenced by the chosen logic style. Depending on the application, the kind of circuit to be implemented, and the design technique used, different performance aspects become important, disallowing the formulation of universal rules for optimal logic styles [1].

This paper analyzes 2-to-1 multiplexer using complementary CMOS, and pass-transistor logic styles. These implementations are compared based on transistor count, power dissipation, and delay

Multiplexer Circuit

A circuit that generates an output that exactly reflects state of one of a number of data inputs, based on value of one or more control inputs is called "multiplexer". A multiplexer with two data inputs is referred as "2-to-1 or2:1" multiplexer. Commonly used circuit and graphical symbol for 2:1 multiplexer is represented in Fig.1.

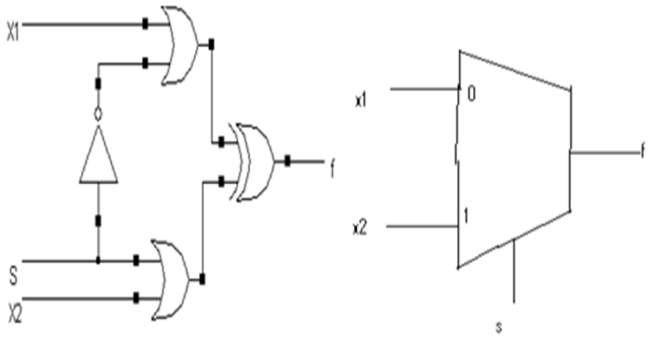

Fig.1. Circuit and Graphical symbol of 2:1 Multiplexer

Logic expression for multiplexer output is given in equation 1.

$$F = \hat{S}\, X1 + SX2 \quad (1)$$

II. LOGIC STYLES

A logic style is the way how a logic function is constructed from a set of transistors. It influences the speed, size, and power dissipation and wiring complexity of a circuit. All these characteristics may vary considerably from one logic style to another and thus make the proper choice of logic style crucial for circuit performance.

a) Complementary CMOS Logic style:

Any logic function in complementary CMOS is realized by NMOS pull-down and PMOS pull-up networks connected between gate, output and power lines [2]. Input signals are connected to transistor gates only. Pseudo NMOS [9] and Cascode Voltage Switch Logic (CVSL) fall under CMOS rationed logic family.

b) Pass-transistor Logic style:

The pass-transistor logic reduces the number of transistors required to implement logic by allowing the primary inputs to drive gate terminals as well as source-drain terminals. The advantage is that one pass-transistor network (either NMOS or PMOS) is sufficient to perform the logic operation [7, 8].

Several pass-transistor logic styles such as NMOS Pass Transistor Logic, Double pass-transistor logic (DPL), CMOS Transmission gate, LEAN Integrated pass gate logic (LEAP) and pass transistor logic(PTL) are considered to implement 2-to-1multiplexer[3,5,6].

Among all these NMOS Multiplexer is optimal. It uses two NMOS transistors and these two-pass transistors at the input select which signal to propagate. The logic levels will be deteriorated by the pass transistor. The threshold voltage of both pass-transistors should be identical for accurate operation.Fig.2 represents design of 2-to-1 multiplexer using several logic styles.

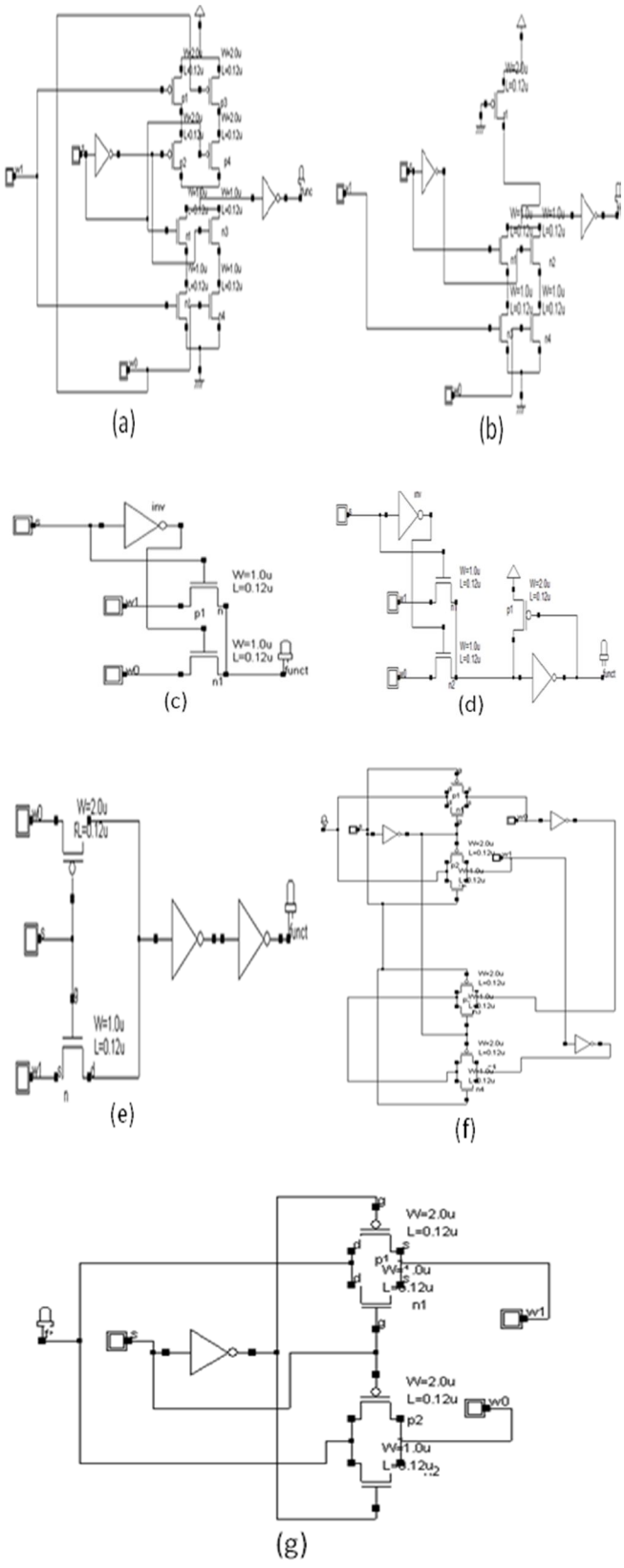

Fig.2. 2-to-1 multiplexer in (a) Static CMOS(b) Pseudo NMOS (c) NMOS (d) LEAP (e)Pass transistor logic (f) DPL (g) CMOS TG.

III. APPLICATIONS

Multiplexers are used to send data from one location to another location. Many tasks in communication control systems and computer systems can be performed by combinational logic circuits. Multiplexer are used to design any digital combinational logic circuit. Multiplexers are used in many applications such as:

- Cross bar switching
- Logic function generator
- Look up tables
- adders

This paper analyzes the cross bar application using multiplexer.

a) Cross bar switching:

In electronics a cross bar switch is a single layered switch connecting multiple inputs to multiple outputs in a matrix form. Its function is to provide a capability to connect any input to any output. Fig 3 shows the architecture of unidirectional cross bar switch.

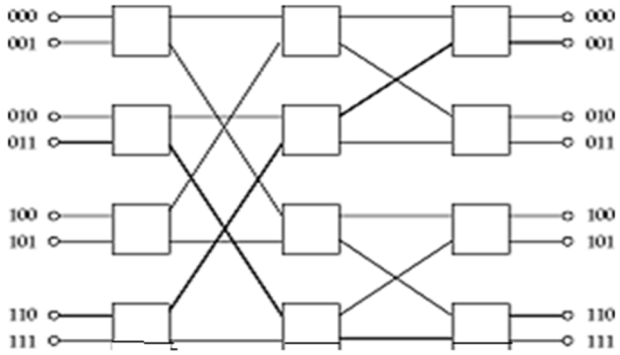

Fig.3 Multiple inputs to multiple outputs cross bar switch

The Fig.4 shows a circuit that has two inputs X1 and X2 and two outputs Y1 and Y2.The function of the circuit is to allow either of the inputs to be connected to the either of the outputs, under the control of another inputs. A circuit that has *n* inputs and *k* outputs whose sole function is to provide a capability to connect any input to any output is referred as *nxk* cross bar switch. Cross bars of various sizes can be created with different number of inputs and outputs. When there are two inputs and two outputs it is called as 2x2 cross bar [4, 5].

Fig. 4 2x2 Cross bar switch

Fig. 5 shows how the cross bar can be implemented using 2x1 multiplexers. The multiplexer select inputs are controlled by the signals. If *S = 0*, the cross bar connects X1 to Y1 and X2 to Y2, while *S = 1*, the cross bar connects X1 to Y2 and X2 to Y1.Cross bar switches are useful in many applications in which it is necessary to be able to connect one set of wires to another set of wires where the connection pattern changes from time to time.

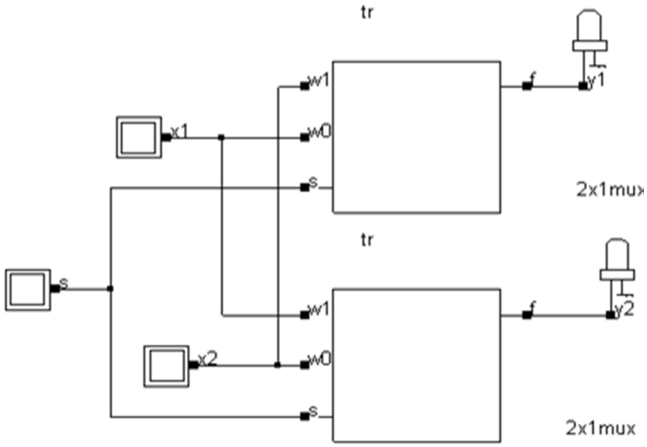

Fig. 5 Implementation of crossbar switch using multiplexers

IV. RESULTS

The different technique implementations of 2x1 Multiplexer were simulated using CAD tools DSCH3 and Micro wind 3.1 in submicron regime. All the schematics were drawn using 65nm technology with a 1 V supply voltage. The calculation of power ,delay, and area were carried out for 2-to-1multiplexer in Static CMOS, 2TMux (pass transistors),CMOS transmission gate, DPL, LEAP NMOS logic style and the values are shown in Table 1.

Table1: Performance of 2 to 1 multiplexer in all the logic styles.

Logic Style	Power Consu-mption (mw)	Delay (ns)	Transi-stor count	Area (μm^2)
CMOS	0.821	0.102	12	118.4

DPL	0.797	0.076	12	117.4
Pseudo	0.308	0.100	9	55.53
NMOS	0.252	0.066	4	17.77
LEAP	0.215	0.076	5	29.15
TR Gate	0.198	0.072	6	43.34
PTL	0.575	0.098	6	31.14

The graphs below show power, delay, area, transistor count, power delay product for different logics.

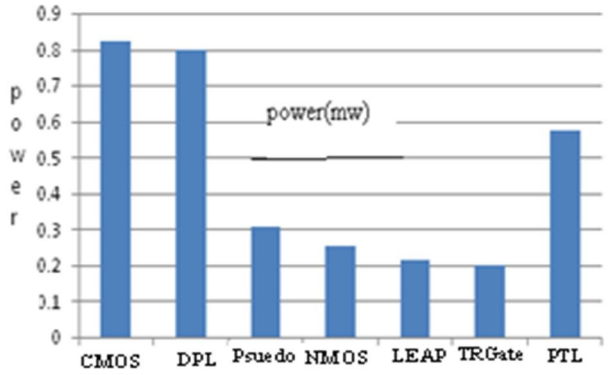

Fig. 6 Logic styles Vs Power consumption for 2-to-1 multiplexer

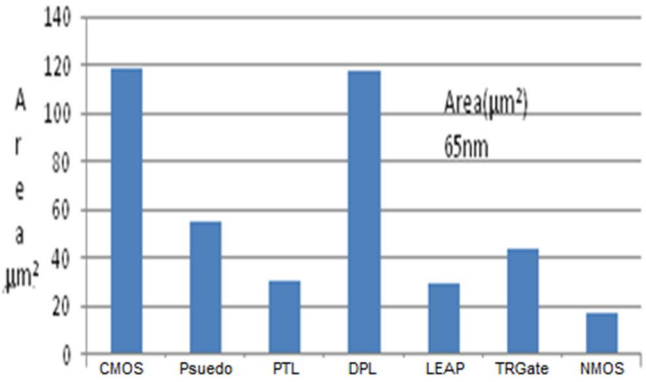

Fig. 7 Logic styles Vs Area for 2-to-1 multiplexer

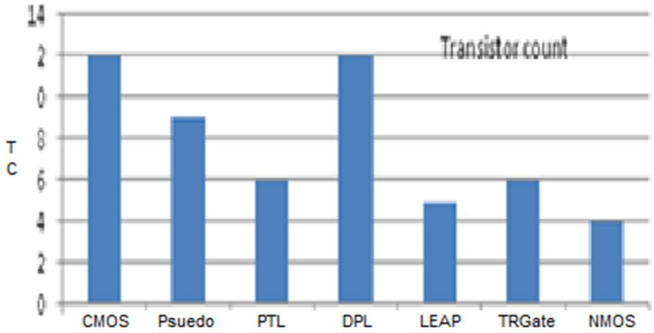

Fig. 8 Logic style Vs Total count of transistors needed for 2-to-1 Multiplexer

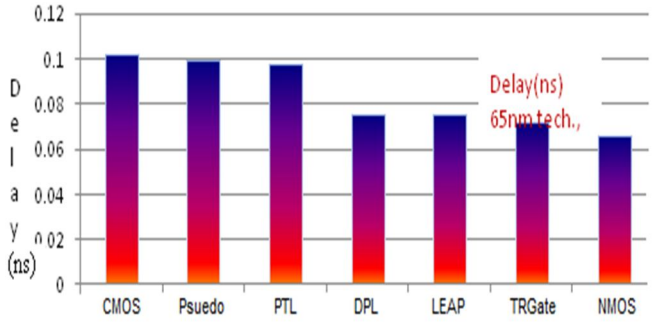

Fig.10. Logic style Vs Delay for 2-to-1 multiplexer

V. CONCLUSIONS

From the work carried out in this paper for implementation of 2 to 1 Multiplexer, we conclude that use of NMOS technology for implementation of 2 to 1 multiplexer provides improvement in power consumption, delay and power delay product when compared with implementation in other techniques like CMOS, Pseudo, PTL, DPL, LEAP, TR Gate which is evident form Table 1.

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