Design of a Low Power and Stable 11T SRAM cell with bit-interleaving capability

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Abstract  A low power and high stable single ended 11T SRAM cell has been proposed with bit-interleaving capability. A column aware scheme is used in the cell to achieve highly stable SRAM cell which exhibit better performance than the previous designs. The proposed design has robust read operation and exhibits lower power consumption and better stability as compared to existing designs. This proposed 11T SRAM has been compared with conventional 6T SRAM cell and 9T SRAM cell in term of Power consumption, Delay and Power Delay Product (PDP) at various supply voltages as 1.8V, 1.6V and 1.4V. For the stability analysis SNM (Static Noise Margin) also analyzed at the supply voltage 1.8V. The simulations of all circuits are done on Cadence Virtuoso at 180nm CMOS technology and the simulation results are analyzed and verify to show that proposed design is better than the existing designs. The proposed 11T SRAM shows the better performances in terms of power consumption and PDP at all the supply voltages. At 1.8V power saving by the proposed design is 73.88% and improvement in PDP is 71.53% compared to standard 6T SRAM cell and significant improvement is observed at other supply voltages also. In term of stability the proposed design showing good result as compare to existing designs.

Keywords SRAM cell, Leakage Power, Low Power, Stability, Bit-interleaving, PDP.

I. INTRODUCTION

Ever since the concept of miniaturization took off, Process voltage and Temperature variations have become the prominent issues because of device scaling. But in the DSM (Deep Submicron Tech) as the size of the CMOS is scaling down; the leakage power is most common issue for SRAM cells which are designed for a low power application. As a result the power consumption in SRAM cell becomes main problem. Low power design of SRAM without compromising with the speed performance becomes the main issue in the modern VLSI designs. Furthermore due to scaling the circuits also faces design challenges for low power SRAM designs. Because of low \( V_{th} \) and ultra-thin gate oxide, the leakage power consumption is increased [1]. The stability of the cell during read, write mode is also affected [2]. The adoption of supply voltage scaling becomes most effective technique for energy saving since it reduces the power consumption of the circuit in significant amount [3]. But with the scaling down of devices and supply voltages, the variability of SRAMs in process variation parameters and threshold voltage together with \( I_{on}-I_{off} \) ratio increase severely and this degrades cell stability by reducing the Static Noise Margin (SNM) [9, 10]. The SNM has linear dependency on the supply voltage, as the supply voltage is scaled down for power reduction the cell stability severely get affected. Hence to get ultra-low power consumption while keeping the cell stability constant becomes the main issue of SRAM designs in this scenario. In this paper, a 11T SRAM cell has been proposed for bit-interleaving application. Some other SRAM cell with bit interleaving have been presented in [4-8] in past. The proposed design has less power consumption, high speed, improved read and write stability, read robustness at the cost of area overhead.

The brief overview of this paper as follows, in section II consist of literature review discussions i.e. standard 6T SRAM and existing 9T SRAM cell has been discussed. Section III elaboration of the proposed work has discussed, section IV contains the simulation results and cell performance analysis discussion and section V consists of conclusion of the whole paper.

II. LITERATURE REVIEW

2.1 Conventional 6T SRAM Cell

The Conventional 6T SRAM cell has combination of six transistors in which four transistors (N3 P1 N4 P2) formed two inverters. These two inverters are back to back connected in cross coupled manner, apart from this two access NMOS transistors N1 and N2 acting as pass transistors and two data storing nodes (Q and QB). These data storing nodes are accessed by the pass transistor N1 and N2 as shown in Fig.1. These back to back connected inverters forming the latch to store the bit. The access transistors are turns on by enabling Word Line (WL). When the Word Line (WL) is low, access transistors are disabled and cell works in hold mode, at this mode read or write operations cannot be
performed, at this state latch can hold bit. When the word line becomes high, access transistors N1 and N2 are enabled, and the read and write operations can be performed [14]. Data is written at node Q through bit line and inverted data is stored at the node QB.

**Fig.1 Conventional 6T SRAM cell**

### 2.2 9T SRAM cell

To design 9T SRAM cell three extra transistors N5, N6, P3 are connected. Transistor N6 is connected between data storing node Q and N1 for the data protection during read operation [11], this transistor N6 prevent the discharging of node Q because it turn off during read, write operation. Transistor (N5, P3) forms a special inverter for AND logic operation [8] to activate local word line (LWL). It also have other input lines i.e. bit line (BL),word line (WL) and provide special Read word line (RWL) for read operation, bit line CBLB have a control on transistor N5 as shown in Fig. 2. This 9T SRAM cell is designed for bit-interleaving application for soft error protection and this design also overcome the problem of write 1 failure which was occurring in 6T SRAM cell. Also exhibit significant improvement in write ability, read robustness, reduces write and leakage power consumption, as well as proves to be better tolerance in process variation [12]. The power consumption, speed and stability of the circuit can be further improved by connecting extra circuitry which is done in the proposed 11T design.

**Fig.2. Existing 9T SRAM cell**

### III. PROPOSED DESIGN

#### 3.1 Proposed 11T SRAM cell

Single ended 11T SRAM cell for bit interleaving application has been proposed, the idea of bit interleaving originate from the differential 8T SRAM cell [10]. Later the same idea is used in read disturb free 9T SRAM cell [12]. The working of the proposed cell is a little bit similar to the 9T SRAM cell with improved performance parameters i.e. less power consumption, high speed, less PDP and high stability at the cost of area. The proposed SRAM cell consist of eleven transistors seven NMOS from N1 - N7 and four PMOS from P1-P4 shown in Fig. 3.

**Fig.3. Proposed 11T SRAM cell**

In the proposed circuit two extra transistors P4 and N7 are connected to improve the cell performances. The transistor N7 is for reducing supply voltage and transistor P4 is work as switching transistor. The operation principle of the proposed 11T SRAM cell is discussed below.
Hold mode:
In hold mode, set the word line (WL) at pre-charge high voltage while RWL signal set at low voltage that leads to transistor N1 & N2 turns off to prevent the access of bit lines, CBLB is set high to turn on transistor N6 as a result data retention is afforded by the cross coupled inverter pair.

Write Mode:
In write operation WL is set at low voltage and CBL signal set to high voltage, hence as a result LWL signal is pre-charged to high value hence data is written through bit-line (BL) to storage nodes (Q & QB) through N1.

Read mode:
During read mode first of all set BL to high voltage, then the read operation start through the special word line RWL. CBL connect to high and the CBLB is connected to low voltage and WL remains at high voltage.

By simulation result we have observed that proposed 11T SRAM cell generates Q and QB output which has proper logic with proper output waveform. The output waveform for proposed 11T SRAM cell is shown in Fig. 4.

3.2 Concept of Bit-interleaving architecture
SRAM architecture has mainly two ways to arrange the words. Shared word line shown in Fig. 5(i) and bit interleaving shown in Fig. 5(ii). In share word line, all the bits of the same words are located next to each other shown in Fig.5. This design is most common because of its simplicity and compactness but the bits are adjacent to each other that cause the probability of multi-bit soft errors is very high. To solve the problem of soft errors the 2nd architecture i.e. bit interleaving architecture is used. A detailed explanation of bit-interleaving concept is explained in [8].

IV. CELL PERFORMANCE ANALYSIS
In this section, cell properties such as SNM, Speed, Power consumption, PDP etc. are compared with the existing design, namely the standard 6T cell and 9T cell. All the existing and proposed circuit is simulated using the tool Cadence Virtuoso at 180nm technology. Power consumption and delay is calculated at different supply voltages 1.8V, 1.6V and 1.4V respectively. We observed that as the supply voltage scale down the power consumption of the SRAM cell also reduces but it also affected cell stability. The size of the transistors is taken to be the same for all transistor of the cell for comparison of different type of SRAM designs.
4.1 Speed and power analysis
The proposed design shows 73.88% reduction in power, 71.53% reduction in PDP at 1.8V with respect to standard 6T SRAM and 9.89% reduction in power, 29.11% reduction in PDP at 1.8V with respect to existing 9T SRAM as shown in table-I. The significant improvement at other voltages can be analysed from the Table-II and Table-III. The proposed circuit has been mainly designed with bit-interleaving capability with better performances compared 9T SRAM in term of power, speed, PDP and stability.

Table I: - Power consumption and Delay of existing and proposed SRAM cell at 1.8V

<table>
<thead>
<tr>
<th>SRAM CELL</th>
<th>Power(µW)</th>
<th>Delay(pS)</th>
<th>PDP (fWS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>6T SRAM</td>
<td>1.504</td>
<td>48.12</td>
<td>72.372</td>
</tr>
<tr>
<td>9T SRAM</td>
<td>0.455</td>
<td>63.88</td>
<td>29.065</td>
</tr>
<tr>
<td>Proposed 11T SRAM</td>
<td>0.410</td>
<td>50.25</td>
<td>20.602</td>
</tr>
</tbody>
</table>

Table II: - Power consumption and Delay of existing and proposed SRAM cell at 1.6V

<table>
<thead>
<tr>
<th>SRAM CELL</th>
<th>Power(µW)</th>
<th>Delay(pS)</th>
<th>PDP (fWS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>6T SRAM</td>
<td>1.099</td>
<td>55.19</td>
<td>60.653</td>
</tr>
<tr>
<td>9T SRAM</td>
<td>0.337</td>
<td>67.89</td>
<td>22.878</td>
</tr>
<tr>
<td>Proposed 11T SRAM</td>
<td>0.307</td>
<td>55.54</td>
<td>17.050</td>
</tr>
</tbody>
</table>

Table III: - Power consumption and Delay of existing and proposed SRAM cell at 1.4V

<table>
<thead>
<tr>
<th>SRAM CELL</th>
<th>Power(µW)</th>
<th>Delay(pS)</th>
<th>PDP (fWS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>6T SRAM</td>
<td>0.756</td>
<td>63.12</td>
<td>47.718</td>
</tr>
<tr>
<td>9T SRAM</td>
<td>0.243</td>
<td>73.90</td>
<td>17.957</td>
</tr>
<tr>
<td>Proposed 11T SRAM</td>
<td>0.225</td>
<td>62.62</td>
<td>14.089</td>
</tr>
</tbody>
</table>

4.2 Stability Analysis
The stability of SRAM cell is defined by static noise margin (SNM); the higher the SNM the better the stability. SNM can be defined “the maximum DC noise voltage that can be tolerate by the cell without changing the output bit or stored bit”. So the cell stability is depends on supply voltage, as supply voltage is reduce the cell become less stable. The most common static approach for measuring the SNM is by using butterfly curves, and this curve can be obtain by dc analysis. The SNM of the SRAM cell is defined as the size of the largest square that can fit into the butterfly curve [10].

4.2.1 Hold stability
The hold stability of the SRAM is defined by the HSNM (Hold SNM). In 9T and proposed 11T cell the butterfly curve appear asymmetrical due to the asymmetrical stored structure. Hence the HSNM equals to the smaller one of the two maximum squares. Butterfly curves for HSNM calculation is shown in Fig. 8.

\[
SNM = \min (SNM_1, SNM_2)
\]

**Fig.8. Statistical butterfly curves of Hold mode**

(a) 6T  (b) 9T  (c) Proposed 11T
4.2.2 Write stability

Write stability of SRAM cell can be analyzed by Write static Noise Margin (WSNM). The definition of the conventional WSNM based on the butterfly curve as shown in Fig.9. More WSNM shows better stability.

![Fig.9. Statistical butterfly curves of write mode](image)

(a) 6T  (b) 9T  (c) Proposed 11T

4.2.3 Read stability

Read stability of SRAM cell also can be analyzed by Read static Noise Margin (RSNM). The definition of the conventional RSNM based on the butterfly curve as shown in Fig.10. More RSNM shows better the read stability.

![Fig.10. Statistical butterfly curves of read mode](image)

(a) 6T  (b) 9T  (c) Proposed 11T

The table IV shown below has the comparative analysis of the different SRAM designs. The table clearly shows that the proposed design is giving better performances in term of stability as compare with existing 6T and 9T SRAM design in all three modes i.e. hold mode, read mode and write mode.

**Table IV:** - SNM of existing and proposed SRAM cell at 1.8V

<table>
<thead>
<tr>
<th>SRAM CELL</th>
<th>HSNM</th>
<th>WSNM</th>
<th>RSNM</th>
</tr>
</thead>
<tbody>
<tr>
<td>6T SRAM</td>
<td>528 mV</td>
<td>460 mV</td>
<td>83 mV</td>
</tr>
<tr>
<td>9T SRAM</td>
<td>516 mV</td>
<td>533 mV</td>
<td>71 mV</td>
</tr>
<tr>
<td>Proposed 11T SRAM</td>
<td>558 mV</td>
<td>583 mV</td>
<td>107 mV</td>
</tr>
</tbody>
</table>

V. CONCLUSIONS

In this paper, a novel 11T SRAM cell with bit-interleaving capability has been proposed. The proposed design shows reduction in power consumption, improvement in the stability and PDP at the cost of area overhead. Analysis of results show that, the proposed 11T SRAM cell is giving better performance in terms of stability, power consumption and PDP with respect to standard 6T SRAM cell and 9T SRAM with bit-interleaving capability. The delay of the circuit is increased slightly at the voltages above 1.6V in comparison with that of standard 6T SRAM cell but PDP of the circuit reduces in significant amount at all the voltages. While significant reduction in both delay and power consumption is observed with respect to 9T SRAM. And proposed design is more stable and robust compared with the existing designs.

REFERENCES


